REMARKS

This application now contains claims 11-13, 17, and 45-54. Claims 1-10, 14-16 and 18-44 have been canceled without prejudice. Also, enclosed is a Petition for a three month extension of time together with the appropriate fee.

The Office Action requested that its response include an affirmation of the provisional election of the invention group comprised of claims 11 through 22 that has previously been made by the applicant in a phone call. The applicants hereby affirm the election of claims 11 through 22 and canceled the nonelected claims 1-10 and 23-44, reserving the right to file a divisional application.

The Office Action objected to the drawings for filing to include the reference number 172 mentioned in page 30 of the specification and stated that a drawing correction is required. In response the applicants would like to point out that it is the specification, rather than the drawings that is in error concerning this reference to "pins 172". The specification intended to refer to "pins 152", as is indicated by the following sentence in which these same pins are referred to as "pins 152". In response, the reference to "pins 172" on page 30 has been amended above to read "pins 152" as originally intended.

The Office Action objected to the drawings because the reference character "114" has been used to designate both "chip 114" and "substrate 114." In response, corrections have been made to FIGS. 11-17, 21-26, and 29-38 to label the

change to the numeral for the substrate from 114 to 115 where numeral 114 occurred for the substrate or to add numeral 115 where the substrate was not labeled. In FIG. 39 the numeral 114A has been replaced with 115A. Applicants enclose herewith a version of the drawings, indicating the changes in red and a complete new set of corrected formal drawings, all without the addition of any new matter.

The specification has been amended to cause all references to substrate 114 or 114A to be replaced by references to substrate 115 or 115A, respectively.

The Office Action objected to the abstract originally filed in this application for exceeding the 150-word limit set by regulation for such abstracts. In response the abstract has been amended to comply with the 150 word limit, as is indicated above.

The Office Action rejected Claims 17-22 under 35 U.S.C. 112, second paragraph because it found the phrase "each such layer" in Claim 17 to be vague. In response Claim 17 has been rewritten so the objected-to phrase "each such layer" now reads "each such electrically conductive layer". A similar amendment has been made to Claim 11. It is hoped that this change removes all of the objected to vagueness.

The Office Action rejected claim 17 under 35 U.S.C. 102(b) as being anticipated by Gorczyca et al. In response Claim 17 has been amended to recite that one or more of its dielectric layers are comprised of latex. Since Gorczyca does not disclose latex dielectric layers, the 102(b)

direct-anticipation rejection against this claim, as amended, is no longer appropriate.

The Office Action indicated, in its discussion of Claims 11-16 and 18, that it considered the use of latex dielectric layers to be obvious. But the applicants believe that latex is substantially different than the thermoplatic, thermoset, and silicon adheasive polymers disclosed in both the Gorczyca and Eichelberger et al. references, and that it would not have been obvious to one or ordinary skill in to art to use it for such a purpose.

This is because latex has very different properties than such polymers. It is much more elastic, compressible, and flexible than such materials. The preferred self-vulcanizing latex recited in the application does not even require temperatures above room temperature to solidify. Furthermore, it was not generally known in the art how to get conductive layers to adhere to a latex layer, but it was know well known in the prior art how to make conductive metals adhere to many of the thermoplatic and thermoset polymers disclosed in the cited references.

For all these reasons it would not have been obvious to a person skilled in the art that it would be practical or desirable to make circuits using latex dielectric layers.

Thus, it is submitted that Claim 17 and all the claims that depend from it are not only novel, but also non-obvious over the prior art of record in this application.

The Office Action rejected claims 11 through 16 under 35 U.S.C. 103(a) over the Eichelberger reference. The Office Action admitted that Eichelberger failed to show the use of latex as a dielectric layer, but claimed it would have been obvious to do so, since it stated that "latex is a known polymer material well suited for the intended use."

The applicants admit that latex is a "known polymer", but polymers form such a huge class of molecules in chemistry, that the mere fact that a prior art reference recites the use of a polymers for a given use does not prevent a new use of all chemicals from that huge generic class from being non-obvious. To hold otherwise would be like claiming that a patent which recited the use of a certain medicine for curing a given disease made obvious the use of any medicine, no matter how unobvious, for curing the same disease.

As is stated above with regard to Claim 17, latex has very different properties from the thermoplastic and thermosetting polymers normally used for dielectric layers in many circuitry. Furthermore it was not well known in the prior art how to adhere conductive traces onto latex layers. The specification of this application spends considerable space (see FIGS. 18 through 24) to explain a method for accomplishing this heretofore difficult task.

Thus, it is respectfully submitted that the recitation of latex dielectric layers recited in Claim 11 makes the teaching of that claim non-obvious.

Since Claims 17 and 11 clearly appear to be non-obvious for the reasons stated above, it is respectfully submitted that they, and all the other claims of this application that depend from one of these two independent claims are also non-obvious, and thus patentable.

The Office Action pointed out that the process limitations in Claims 14 through 16 and 20 though 22 carry little weight in claim drawn to structure. In response these claims have been deleted, and new claims 45 through 54, have been added to recite structural differences that result in circuitry which is made by some of the process steps recited in those deleted claims and in the specification. The limitations of these claims are all supported in the specification as filed and do not contain new matter.

The prior art made of record but relied upon does not appear, from a quick review, to contradict any of the arguments for patentability made above.

If the Examiner has any further questions, and feels a telephone interview may be helpful, he is invited to call the undersigned attorney.

Since he number of additional claims in this application falls within the number of claims already paid for, not further fee are required beyond the fee for the extension of time. However, in the event additional fees are required or a credit need be given, please charge any deficiencies to or credit any overpayment to Deposit Account No. 03-2410, Order No. 12569-107

Based on the above discussion it is respectfully submitted that all of the remaining claims in this application, that is Claims 11 through 13, 17, and 45 through 54, are patentable, and allowance of these claims is respectfully requested.

Respectfully Submitted On
Behalf Of Applicants,

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12569-107-RespOA

APPENDIX TO
AMENDMENT IN RESPONSE TO
FIRST OFFICE ACTION
WITH AMENDED TEXT
MARKED TO SHOW CHANGES

AMENDMENTS TO Please amend paragraphS IN THE SPECIFICATION MARKED TO SHOW CHANGES

Please amend paragraph 90

Returning now to the embodiment of the invention using the frame 100 of the type shown in Fig. 1, once the epoxy 118 has been placed on the back of the chips as shown in Fig. 6, the assembly comprising the glass substrate 110, the dicing tape 112, and the frame 100, including the chips which been mounted within it, is aligned with a bottom substrate ~~114~~115. This alignment can be aided by looking through the glass substrate 110 and through via holes 106 to seek alignment with conductively filled vias 117. Such alignment can also be aided by the use of fiduciary marks on the substrate ~~114~~ 115 and/or the frame 100 that are to be aligned.

Please amend paragraph 91

In the embodiment shown in Fig. 11 the substrate ~~114~~ 115 is a ball grid pad which has a plurality of vias 117 filled with conductive material, and gold plated ball grid pads 119 on its bottom surfaces. Normally the substrate will be a large sheet having a shape and area similar to both the plastic sheet containing the frames 100 and the substrate 110.

Please amend paragraph 93

As shown in Fig. 39 a substrate, such as the substrate ~~114A~~ 115A shown in that figure, can have passive components formed on it before it is joined with the chips 114 and 116. In Fig. 39 these passive components include a thin film resistor 120 and a thin film capacitor 122.

Please amend paragraph 94

Fig. 12 illustrates the assembly after the frame 100 and the chips it is holding have been bonded to the substrate ~~114~~114. The pressure of the bottom substrate ~~114~~ 115 against the epoxy 118 ~~fans~~tends to force portions of that epoxy into the gaps between the chips and the frame 100, which helps to further bond those chips in place relative to the frame.

Please amend paragraph 97

Once the vias 106 have been filled with conductive material and the assembly has been heated to help that epoxy harden and become more conductive, a layer of liquid la~~ shown in~~ tex 126 is evenly spread across the top of the assembly. This is done by its spinning, in which centrifugal force is used to spread material across a surface. In some embodiments of the invention, this latex is a self-Vulcanizing latex, such as is sold by Haveatext, Inc.

Please amend paragraph 98

After the ~~epoxy~~ latex 126 has had been hardened, a layer of photoresist 128 is deposited upon it and pattern by photolithographic techniques so as to create gaps 130 in that photoresist which leave portions of the latex surface 128 through which via holes are to be formed uncovered. The bonding pads on the integrated circuits 114 and 116 and via holes 106 over which the via holes are to be made in the latex layer 126 are large enough and far enough apart, and their position is sufficiently exactly known because of the relative rigidity of the frame ~~inaccuracy~~ and the accuracy of the positioning of the integrated circuits, that it is relatively easy to correctly locate via holes over them in the latex layer 126 when performing wafer scale photolithography without being able to see through the latex layer 126.

Please amend paragraph 99

Once this is been done the assembly shown in Fig. 15 is submitted to a reactive ion etch represented by the vertical arrows 132. A reactive ion etch is one in which chemically reactive ions are rapidly moved back and forth ~~line~~ in an oscillating electromagnetic field in a direction generally perpendicular to the surface being etched, so that they will collide with that surface with considerable energy, which enhances their etching chemical reaction with the material of that surface.

Please amend paragraph 101

Fig. 16 illustrates the assembly of Fig. 15 after the ion ~~edge~~ etch has ended, and after the photoresist has been

removed. As can be seen from this figure, after this process the latex layer 126 has had holes 134 etched through it in those locations which correspond to the openings 130 in the photoresist shown in Fig. 15. The purpose of these holes is to~~o~~ etch~~ed~~ down to the bonding pads of the integrated circuits 114 and 116 and the top of the conductive via holes 106.

Please amend paragraph 107

In other embodiments of the invention the ~~talus~~ catalytic particles used ~~to be~~are made of any metal in the eighth group on periodic table. This group includes cobalt, palladium, ruthenium, rhodium, platinum, iridium, osmium, nickel, and iron.

Please amend paragraph 122

29 the assembly of Fig. 28 is flipped upside-down so the chips 114 and 116 can be mounted upon a substrate ~~114~~115, which can be of the same types of substrates described above with regard to Fig. 11.

Please amend paragraph 123

Once the epoxy 118 has had a chance to firmly bond chips 114 and 116 to the substrate ~~114~~115, the dicing tape 112 is exposed to radiation through the glass 110. This causes the dicing tape to lose its adhesive characteristic, freeing the assembly shown in Fig. 30 from the glass substrate and the dicing tape.

Please amend paragraph 124

Then a layer of liquid latex 126B is placed over the substrate ~~114~~ 115 in sufficient thickness to cover the tops of the chips 114 and 116. A third substrate 150 is position so that pins ~~172~~ 152 will push via holes into the latex 126B. The surface of the substrate 150 facing the latex and the surface of its pins 152 are covered with Teflon so that they will not stick to the latex.

Please amend paragraph 125

In Fig. 32 the substrate 150 and its pins 152 are shown pressed against the latex layer 126B so as to flatten out that layer and to cause the pins 152 to extend substantially all the way down to the top surface of the substrate ~~114~~115.

Please amend paragraph 126

Once the latex layer 126B has had a chance to cure, the substrate 150 and its pins 152 are removed from the assembly of Fig. 32, leaving the assembly as shown in Fig. 33. In this assembly the top of the latex layer 126B is close to being coplanar with tops of the chips 114 and 116. In addition via holes 106A have been formed in the layers 126B which connect down to the vias 117 contained in the substrate ~~114~~115.

Please amend paragraph 129

Fig. 35 illustrates the assembly after the via holes A have been filled with conductive material, such as the conductive

epoxy 118 which is also used to attach the chips 114 and 116 to the substrate ~~114~~115.

Please amend paragraph 133

Fig. 39 is an illustration of a multichip module which is similar to that shown in Fig. 38 except that in its the copper see layers are not separately shown and the substrate ~~114A~~ 115A shown in Fig. 39 has had passive components formed on its surface before was attached to the integrated circuits 114 and 116. These components include a thin film resistor 120 and a thin film capacitor 122.

Please amend paragraph 136

The aspects of the present invention relating to the use of metal seed particles to aid in electroless plating are applicable to the plating of metals other than copper. In fact this technique can be used in combination with a deposition of almost any metal which can be deposited by electroless plating. In aspects of the invention which ~~were to the~~ use ~~of~~ both a dielectric material and a conductive layer made of material which are relatively flexible, the combination of latex dielectric and a copper conductive layer is a relatively beneficial want because both materials are relatively flexible, and copper is an extremely good conductor.

AMENDMENTS TO CLAIMS MARKED TO SHOW CHANGES

-11. (Amended) An electrical circuit comprised of:
-one or more dielectric layers comprised of latex; and
-one or more layers of electrically conductive material patterned to form multiple electrical interconnects, with each such electrically conductive layer placed on top of one of said dielectric layers.

-17. (Amended) A multichip module comprising:
-a plurality of integrated circuits mounted on a substrate;
-one or more flexible dielectric layers comprised of ~~a flexible dielectric material~~latex; and
-one or more layers of electrically conductive material patterned to form multiple electrical interconnects between bonding pads on different ones of said integrated circuits, with each such electrically conductive layer placed on top of one of said dielectric layers.

AMENDMENT TO ABSTRACT MARKED TO SHOW CHANGES

An electrical circuit having one or more dielectric layers formed of latex; and one or more layers of electrically conductive material, such as copper, patterned to form multiple electrical interconnects, with each such layer placed on top of one of said dielectric layers. The dielectric and conductive layers can be used to connect multiple chips in a multichip module. The latex layers can be formed to have a top surface that contains peaks and valleys, and the conductive layers can be formed of a first metal that substantially fills such valleys, so as to increase the adherence of the metal to the latex surface. The layers of conductive metal can contain particles of a second metal between said peaks and valleys of the latex layer that were used as a catalytic seed particles to promote the deposition of the metal layer onto the top surface of the latex.

~~A method for plating metal on a dielectric material includes dipping the dielectric in a solution containing catalytic metal particles. These particles have a dipole which helps them attach to the dielectric's surface. The dielectric's surface can be roughened to make it more attractive to such particles. The dielectric material is then placed in a metal salt solution that causes metal to be plated upon the dielectric by electroless plating. A thicker metallic layer can be deposited on top of the resulting layer by electroplating. This or other methods can be used to make an electrical circuit having one or more dielectric layers comprised of latex and one or more layers of conductive leads. A multichip module can be made which includes a plurality of integrated circuits mounted on a substrate; one or more dielectric layers comprised of a flexible dielectric material; and one or more layers of electrically conductive material patterned to interconnect such ICs. Such a module can be manufactured by placing a frame, with holes for holding integrated circuits, against a flat substrate. Integrated circuit chips are placed through the frame's holes to planarize their top surfaces against the flat substrate. The flat substrate is removed. One or more layers of dielectric are placed on top of the frames and chips. Photolithographic techniques are used to create conductive paths on the dielectric material between the ICs. The multichip module can also be manufactured by a similar process that does not use such frames.~~

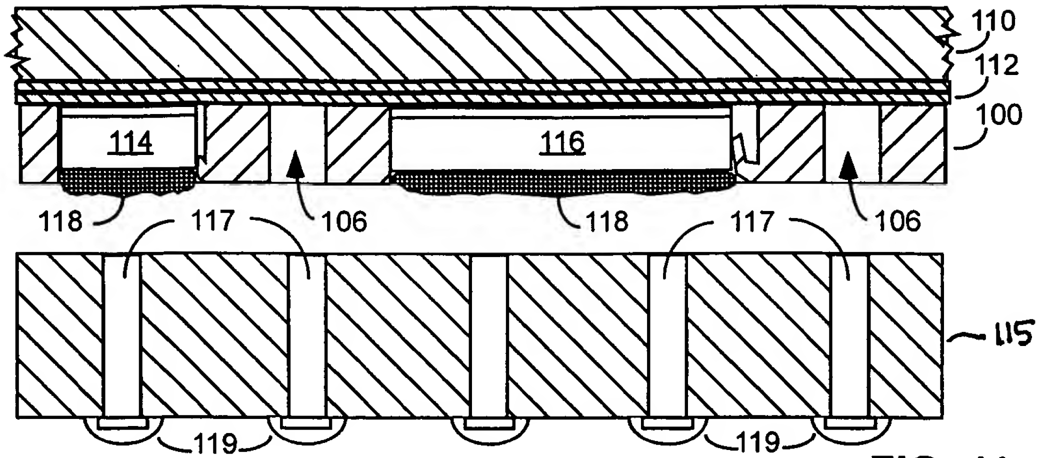

FIG. 11

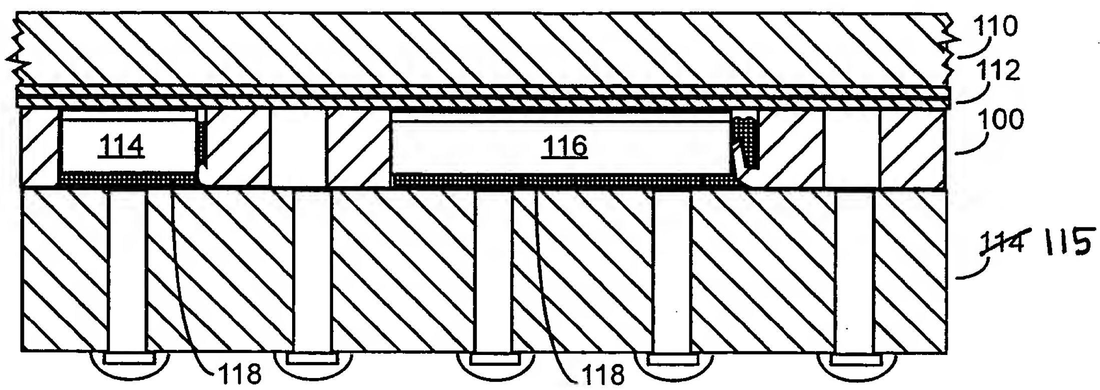

FIG. 12

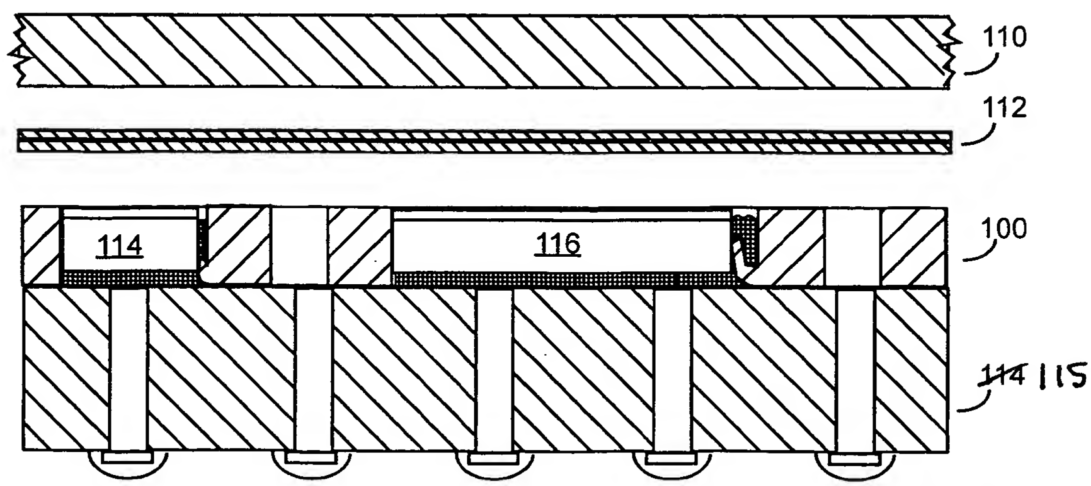

FIG. 13

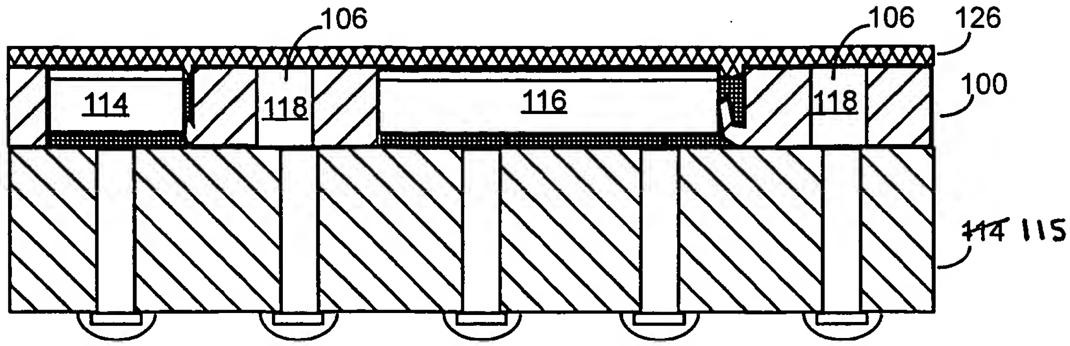

FIG. 14

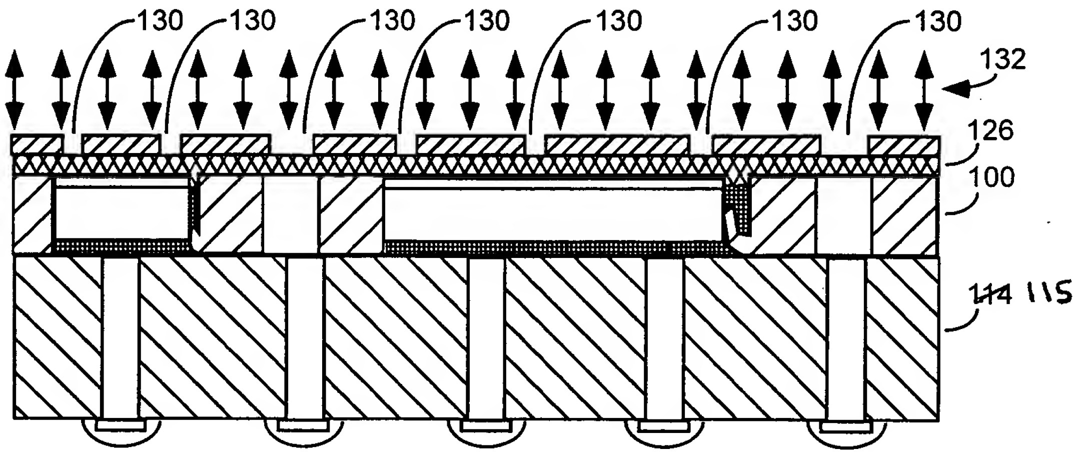

FIG. 15

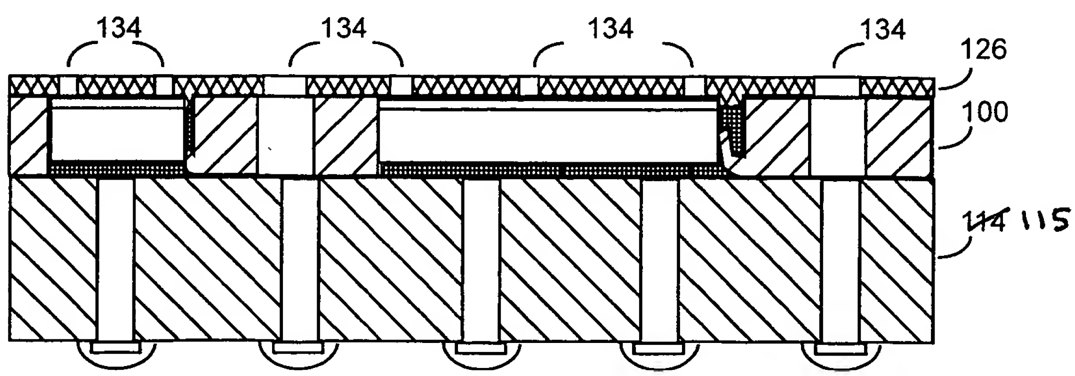

FIG.16

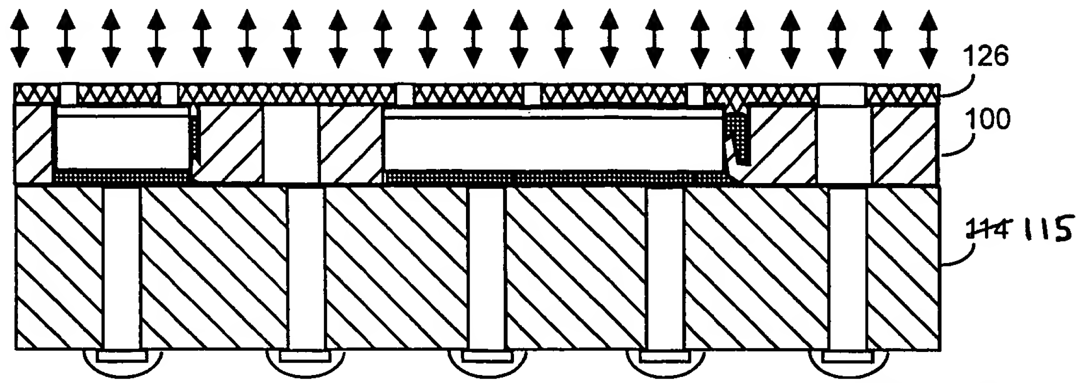

FIG. 17

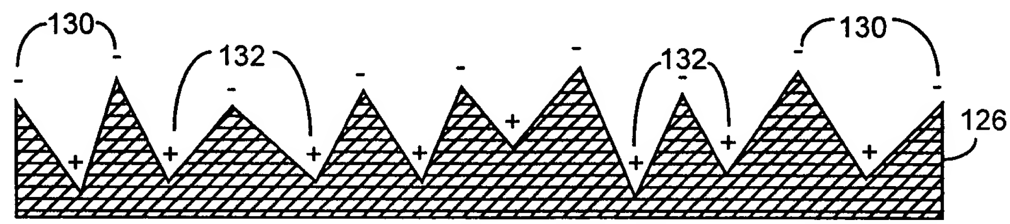

FIG. 18

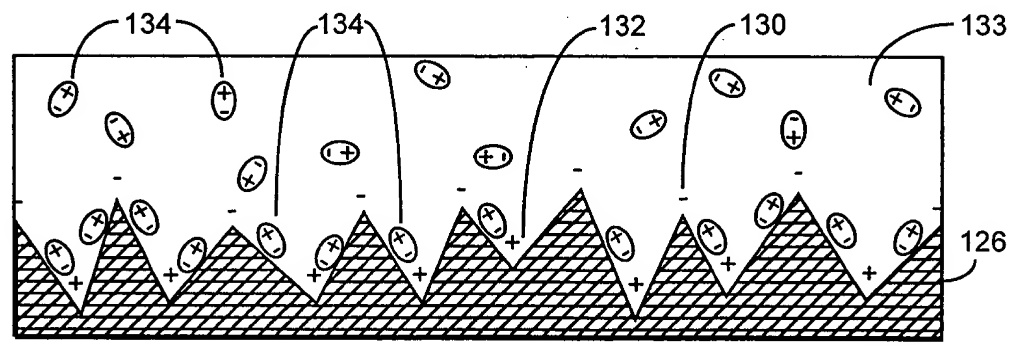

FIG. 19

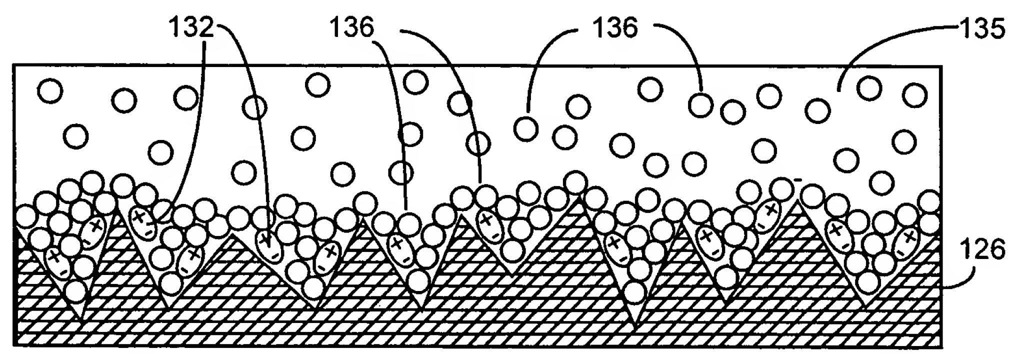

FIG. 20

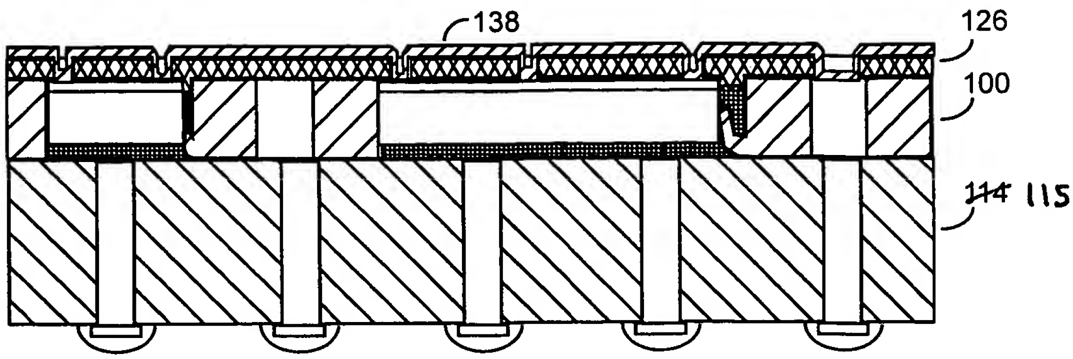

FIG. 21

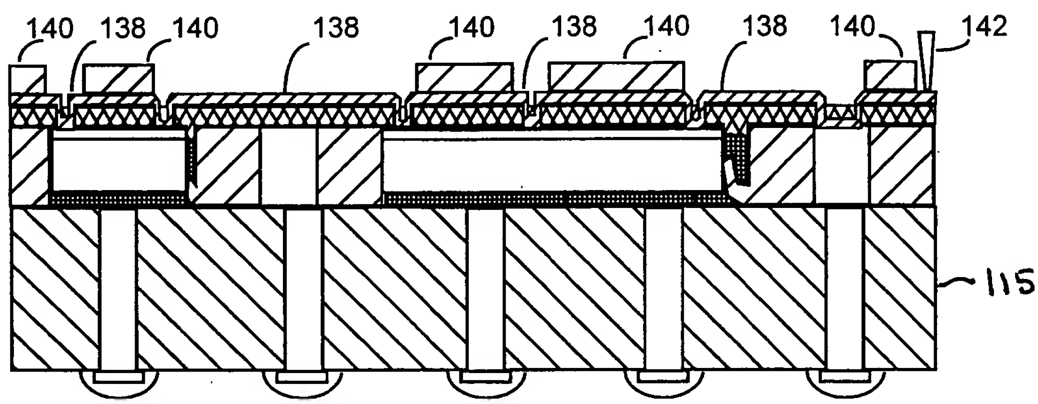

FIG. 22

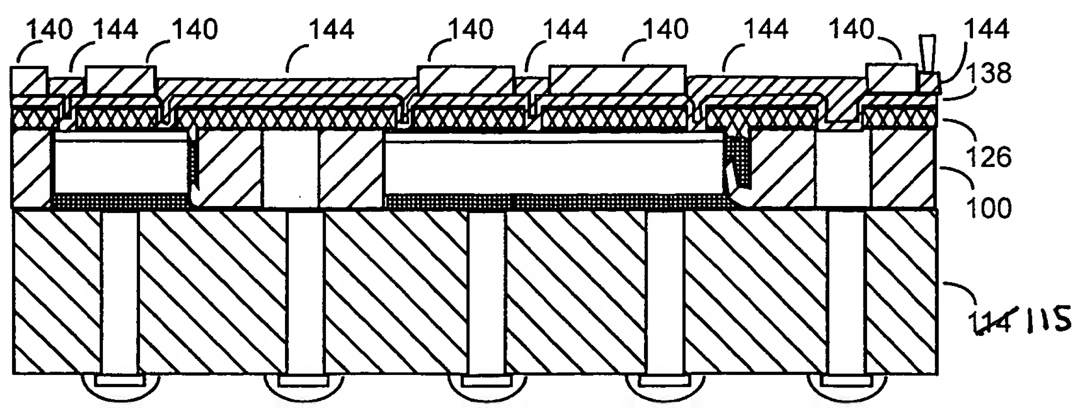

FIG. 23

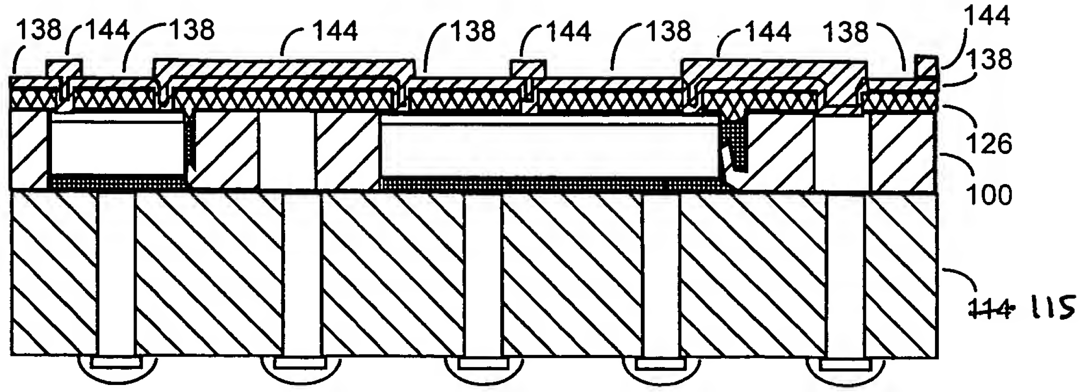

FIG. 24

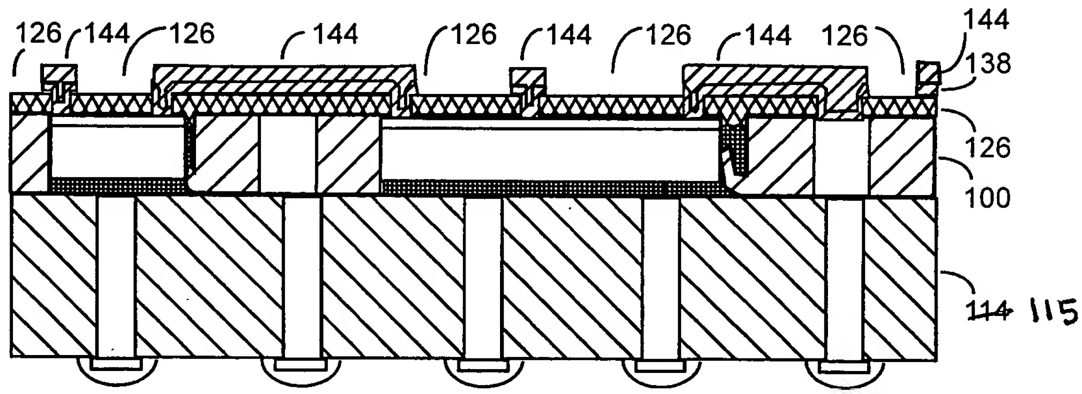

FIG. 25

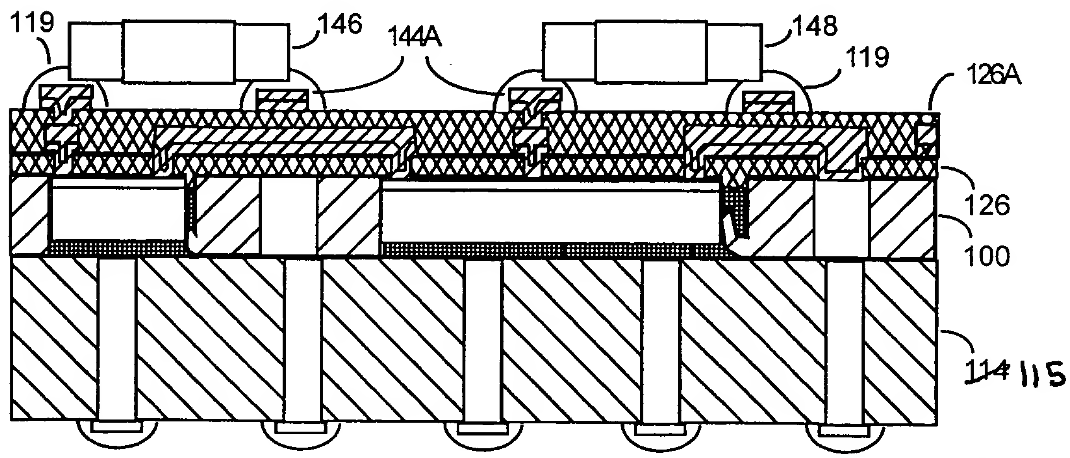

FIG. 26

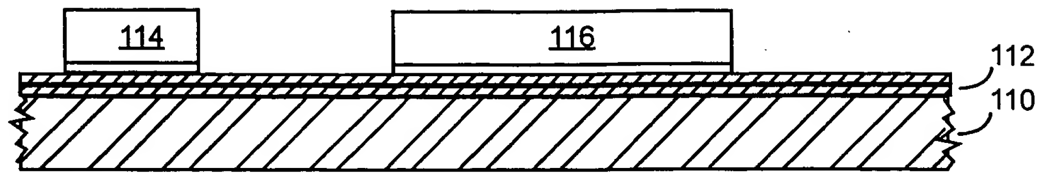

FIG. 27

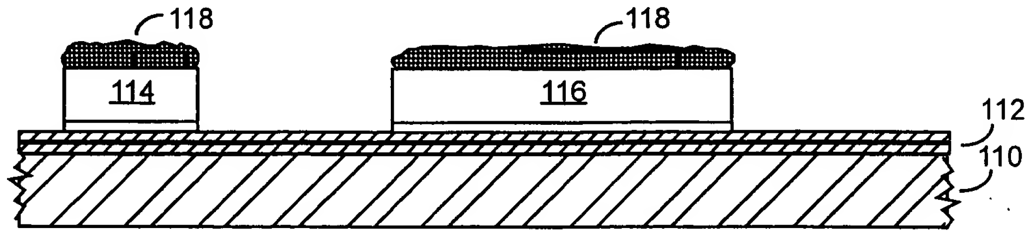

FIG. 28

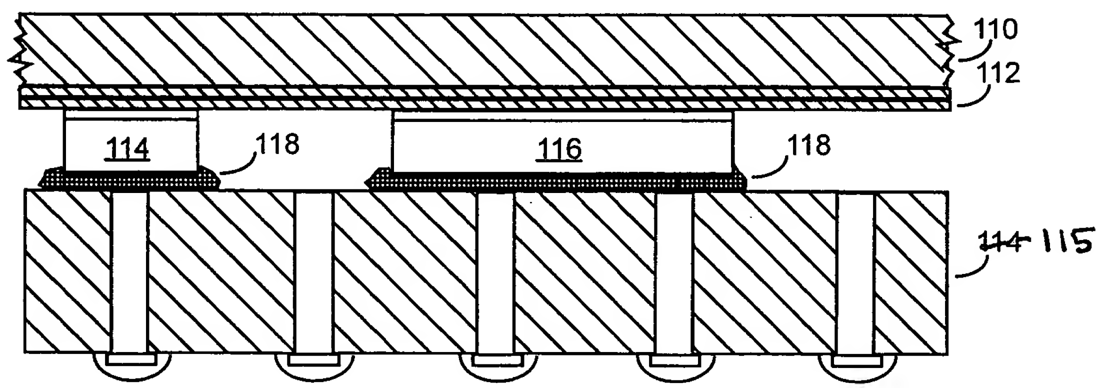

FIG. 29

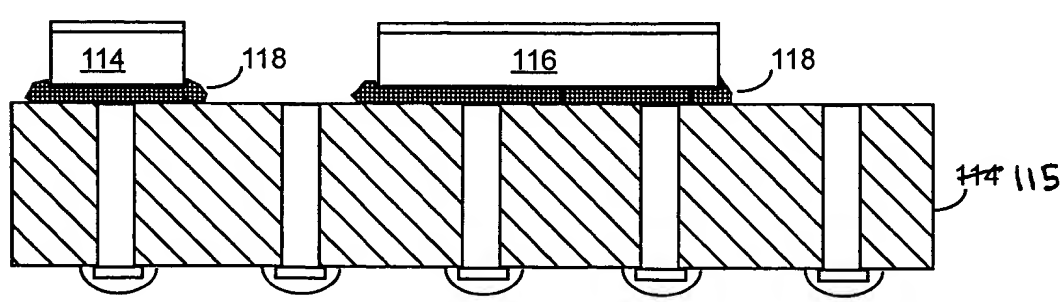

FIG. 30

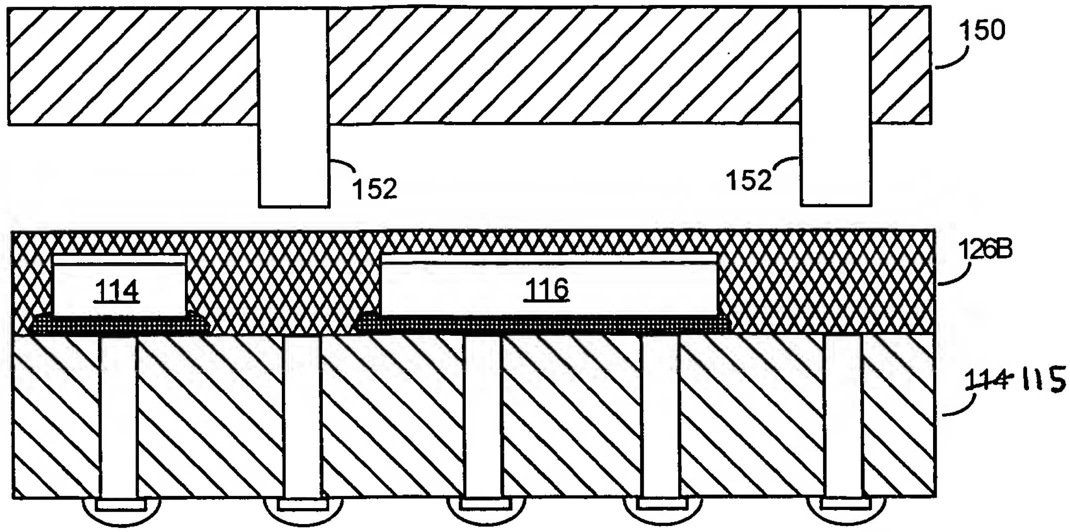

FIG. 31

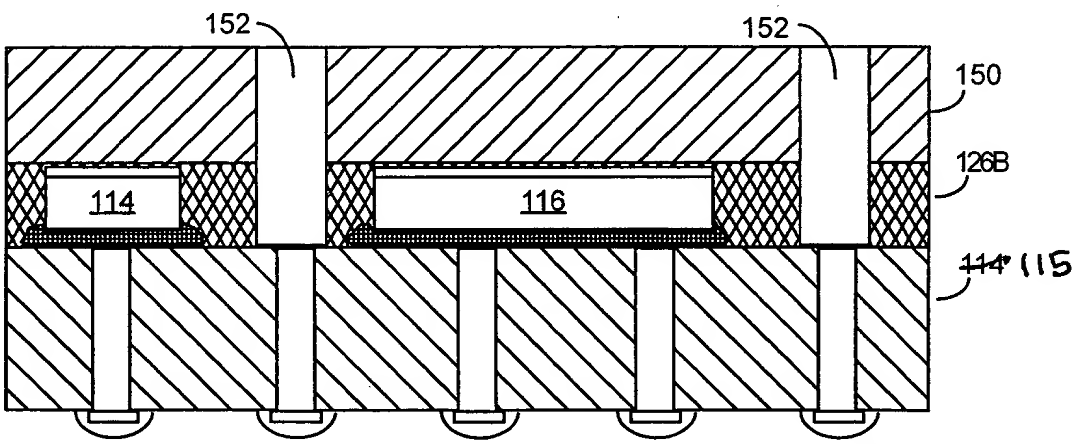

FIG. 32

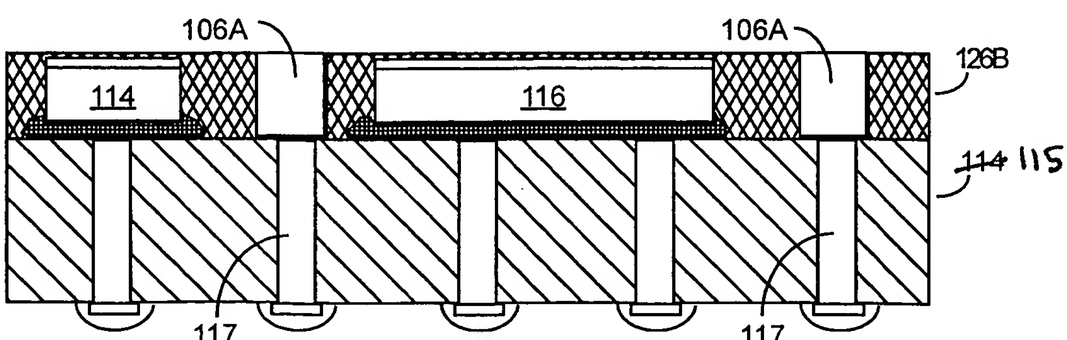

FIG. 33

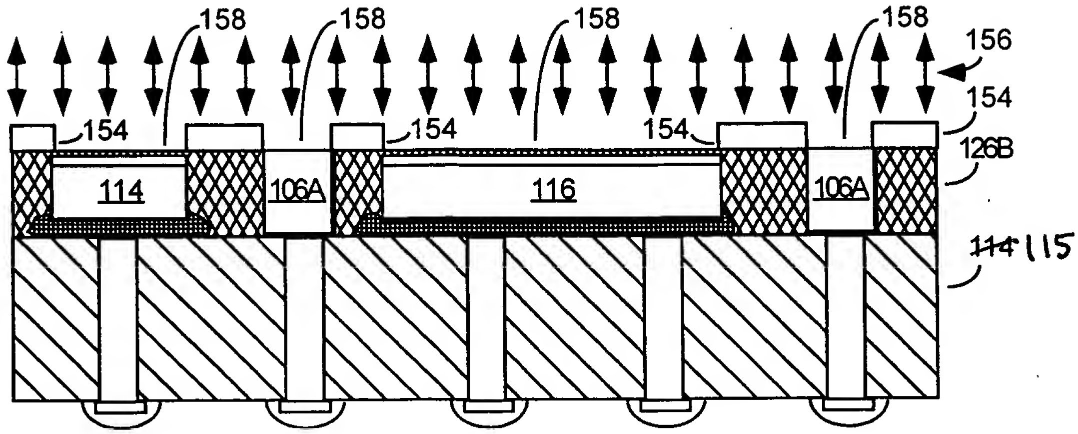

FIG. 34

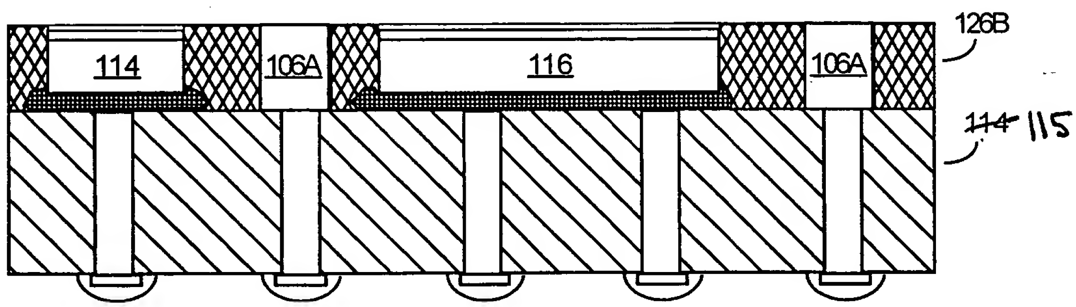

FIG. 35

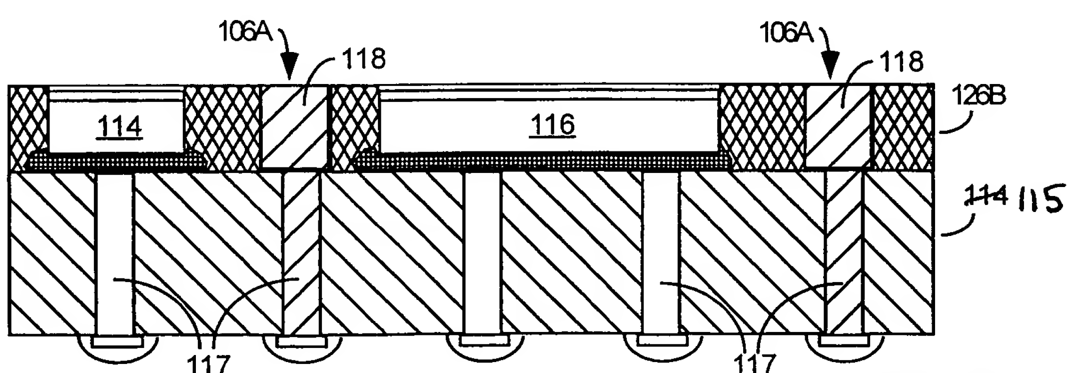

FIG. 36

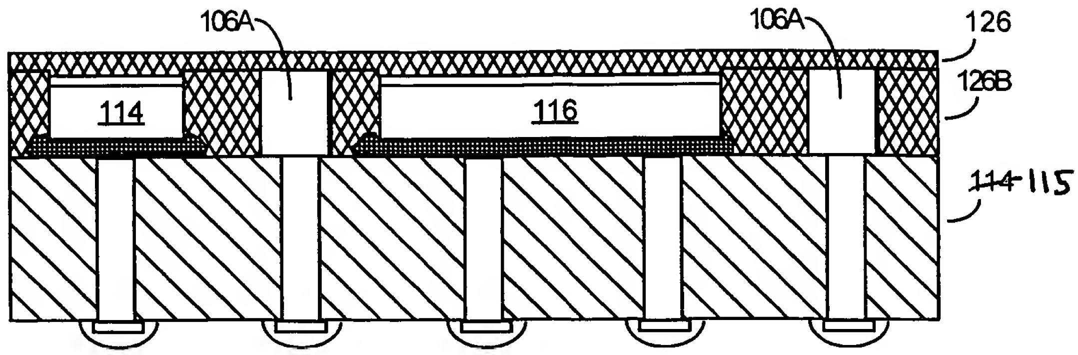
106A
106A
126
126B
114
116
~~114~~ 115

FIG. 37

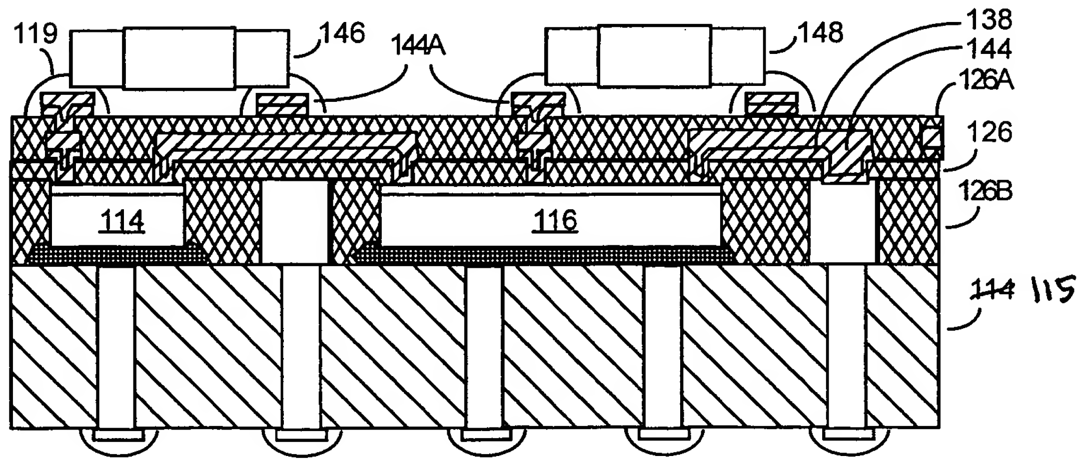
119
146
144A
148
138
144
126A
126
126B
114
116
~~114~~ 115

FIG. 38

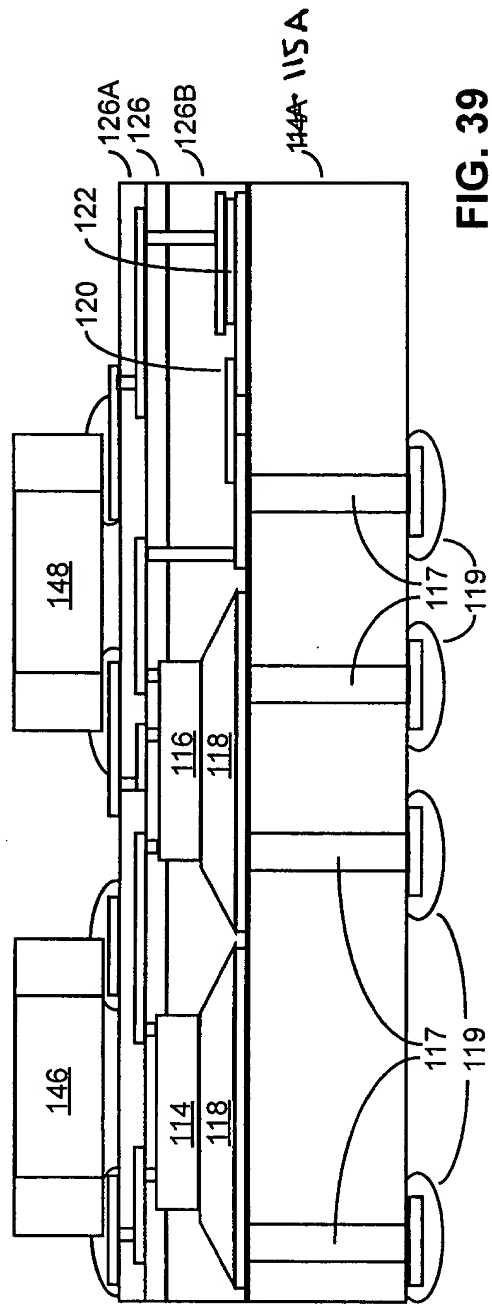
126A
126
126B
~~114A~~ 115A
122
120
148
116
118
146
114
118
117
119
117
119

FIG. 39